1. A circuit comprising a dual differential-input amplifier that comprising the following:

a first PMOSFET having a source terminal coupled to a high voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal;

a second PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal, and having a gate terminal;

a third PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal coupled to the gate terminal of the second PMOSFET, and having a gate terminal coupled to the drain terminal of the third PMOSFET;

a fourth PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal of the fourth PMOSFET;

a fifth PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal, and having a gate terminal coupled to the gate terminal of the fourth PMOSFET;

a sixth PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal coupled to an output terminal of the dual differential-input amplifier, and having a gate terminal coupled to the gate terminal of the first PMOSFET;

a first NMOSFET having a source terminal coupled to a low voltage source, having a drain terminal coupled to the drain terminal of the first PMOSFET, and having a gate terminal coupled to the drain terminal of the second PMOSFET;

a second NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal of the second NMOSFET and to the drain terminal of the second PMOSFET;

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a third NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal of the third NMOSFET and to the drain terminal of the fifth PMOSFET;

a fourth NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal coupled to the output terminal of the dual differential-input amplifier, and having a gate terminal coupled to the drain terminal of the fifth PMOSFET;

a fifth NMOSFET having a source terminal coupled to a current sink, having a drain terminal coupled to the drain terminal of the third PMOSFET, and having a gate terminal coupled to a first input terminal of the dual differential-input amplifier;

a sixth NMOSFET having a source terminal coupled to the current sink, having a drain terminal coupled to the drain terminal of the fourth PMOSFET, and having a gate terminal coupled to a second input terminal of the dual differential-input amplifier;

a seventh PMOSFET having a source terminal coupled to a current source that provides a current of approximately equal magnitude to a current drawn by the current sink, having a drain terminal coupled to the drain terminal of the second NMOSFET, and having a gate terminal coupled to the second input terminal of the dual differential-input amplifier; and

an eighth PMOSFET having a source terminal coupled to the current source, having a drain terminal coupled to the drain terminal of the third NMOSFET, and having a gate terminal coupled to the first input terminal of the dual differential-input amplifier.

2. A circuit in accordance with Claim 1, further comprising an inverter that comprises the following:

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a ninth PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal coupled to an output terminal of a comparator, and having a gate terminal coupled to the output terminal of the dual differential-input amplifier; and

a seventh NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal coupled to the output terminal of the comparator, and having a gate terminal coupled to the output terminal of the dual differential-input amplifier.

3. A circuit in accordance with Claim 2, further comprising the following:

a cascoded PMOSFET coupled between the sixth PMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

4. A circuit in accordance with Claim 3, further comprising the following:

a cascoded NMOSFET coupled between the fourth NMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

5. A circuit in accordance with Claim 2, further comprising the following:

a cascoded NMOSFET coupled between the fourth NMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

6. A circuit in accordance with Claim 1, further comprising the following:

a cascoded PMOSFET coupled between the sixth PMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

7. A circuit in accordance with Claim 6, further comprising the following:

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a cascoded NMOSFET coupled between the fourth NMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

8. A circuit in accordance with Claim 1, further comprising the following:

a cascoded NMOSFET coupled between the fourth NMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

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9. A circuit comprising a dual differential-input amplifier that comprising the following:

a first NMOSFET having a source terminal coupled to a low voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal;

a second NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal, and having a gate terminal;

a third NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal coupled to the gate terminal of the second NMOSFET, and having a gate terminal coupled to the drain terminal of the third NMOSFET;

a fourth NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal of the fourth NMOSFET;

a fifth NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal, and having a gate terminal coupled to the gate terminal of the fourth NMOSFET;

a sixth NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal coupled to an output terminal of the dual differential-input amplifier, and having a gate terminal coupled to the gate terminal of the first NMOSFET;

a first PMOSFET having a source terminal coupled to a high voltage source, having a drain terminal coupled to the drain terminal of the first NMOSFET, and having a gate terminal coupled to the drain terminal of the second NMOSFET;

a second PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal of the second PMOSFET and to the drain terminal of the second NMOSFET;

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a third PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal, and having a gate terminal coupled to the drain terminal of the third PMOSFET and to the drain terminal of the fifth NMOSFET;

a fourth PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal coupled to the output terminal of the dual differential-input amplifier, and having a gate terminal coupled to the drain terminal of the fifth NMOSFET;

a fifth PMOSFET having a source terminal coupled to a current source, having a drain terminal coupled to the drain terminal of the third NMOSFET, and having a gate terminal coupled to a first input terminal of the dual differential-input amplifier;

a sixth PMOSFET having a source terminal coupled to the current source, having a drain terminal coupled to the drain terminal of the fourth NMOSFET, and having a gate terminal coupled to a second input terminal of the dual differential-input amplifier;

a seventh NMOSFET having a source terminal coupled to a current sink that draws a current of approximately equal magnitude to a current supplied by the current source, having a drain terminal coupled to the drain terminal of the second PMOSFET, and having a gate terminal coupled to the second input terminal of the dual differential-input amplifier; and

an eighth NMOSFET having a source terminal coupled to the current sink, having a drain terminal coupled to the drain terminal of the third PMOSFET, and having a gate terminal coupled to the first input terminal of the dual differential-input amplifier.

10. A circuit in accordance with Claim 9, further comprising an inverter that comprises the following:

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a ninth NMOSFET having a source terminal coupled to the low voltage source, having a drain terminal coupled to an output terminal of a comparator, and having a gate terminal coupled to the output terminal of the dual differential-input amplifier; and

a seventh PMOSFET having a source terminal coupled to the high voltage source, having a drain terminal coupled to the output terminal of the comparator, and having a gate terminal coupled to the output terminal of the dual differential-input amplifier.

11. A circuit in accordance with Claim 10, further comprising the following:

a cascoded NMOSFET coupled between the sixth NMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

12. A circuit in accordance with Claim 11, further comprising the following:

a cascoded PMOSFET coupled between the fourth PMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

13. A circuit in accordance with Claim 10, further comprising the following:

a cascoded PMOSFET coupled between the fourth PMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

14. A circuit in accordance with Claim 9, further comprising the following:

a cascoded NMOSFET coupled between the sixth NMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

15. A circuit in accordance with Claim 14, further comprising the following:

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a cascoded PMOSFET coupled between the fourth PMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

16. A circuit in accordance with Claim 9, further comprising the following:

a cascoded PMOSFET coupled between the fourth PMOSFET and the output terminal of the dual differential-input amplifier in a cascoded configuration.

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17. A circuit comprising a dual differential-input amplifier that comprising the following:

a first PNP bipolar transistor having an emitter terminal coupled to a high voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal;

a second PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal, and having a body terminal;

a third PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal coupled to the body terminal of the second PNP bipolar transistor, and having a body terminal coupled to the collector terminal of the third PNP bipolar transistor;

a fourth PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal of the fourth PNP bipolar transistor;

a fifth PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal, and having a body terminal coupled to the body terminal of the fourth PNP bipolar transistor;

a sixth PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal coupled to an output terminal of the dual differential-input amplifier, and having a body terminal coupled to the body terminal of the first PNP bipolar transistor;

a first NPN bipolar transistor having an emitter terminal coupled to a low voltage source, having a collector terminal coupled to the collector terminal of the first PNP bipolar

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transistor, and having a body terminal coupled to the collector terminal of the second PNP bipolar transistor;

a second NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal of the second NPN bipolar transistor and to the collector terminal of the second PNP bipolar transistor;

a third NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal of the third NPN bipolar transistor and to the collector terminal of the fifth PNP bipolar transistor;

a fourth NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal coupled to the output terminal of the dual differential-input amplifier, and having a body terminal coupled to the collector terminal of the fifth PNP bipolar transistor;

a fifth NPN bipolar transistor having an emitter terminal coupled to a current sink, having a collector terminal coupled to the collector terminal of the third PNP bipolar transistor, and having a body terminal coupled to a first input terminal of the dual differential-input amplifier;

a sixth NPN bipolar transistor having an emitter terminal coupled to the current sink, having a collector terminal coupled to the collector terminal of the fourth PNP bipolar transistor, and having a body terminal coupled to a second input terminal of the dual differential-input amplifier;

a seventh PNP bipolar transistor having an emitter terminal coupled to a current source that provides a current of approximately equal magnitude to a current drawn by the

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current sink, having a collector terminal coupled to the collector terminal of the second NPN bipolar transistor, and having a body terminal coupled to the second input terminal of the dual differential-input amplifier; and

an eighth PNP bipolar transistor having an emitter terminal coupled to the current source, having a collector terminal coupled to the collector terminal of the third NPN bipolar transistor, and having a body terminal coupled to the first input terminal of the dual differential-input amplifier.

18. A circuit in accordance with Claim 17, further comprising an inverter that comprises the following:

a ninth PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal coupled to an output terminal of a comparator, and having a body terminal coupled to the output terminal of the dual differential-input amplifier; and

a seventh NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal coupled to the output terminal of the comparator, and having a body terminal coupled to the output terminal of the dual differential-input amplifier.

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19. A circuit comprising a dual differential-input amplifier that comprising the following:

a first NPN bipolar transistor having an emitter terminal coupled to a low voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal;

a second NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal, and having a body terminal;

a third NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal coupled to the body terminal of the second NPN bipolar transistor, and having a body terminal coupled to the collector terminal of the third NPN bipolar transistor;

a fourth NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal of the fourth NPN bipolar transistor;

a fifth NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal, and having a body terminal coupled to the body terminal of the fourth NPN bipolar transistor;

a sixth NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal coupled to an output terminal of the dual differential-input amplifier, and having a body terminal coupled to the body terminal of the first NPN bipolar transistor;

a first PNP bipolar transistor having an emitter terminal coupled to a high voltage source, having a collector terminal coupled to the collector terminal of the first NPN bipolar

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transistor, and having a body terminal coupled to the collector terminal of the second NPN bipolar transistor;

a second PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal of the second PNP bipolar transistor and to the collector terminal of the second NPN bipolar transistor;

a third PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal, and having a body terminal coupled to the collector terminal of the third PNP bipolar transistor and to the collector terminal of the fifth NPN bipolar transistor;

a fourth PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal coupled to the output terminal of the dual differential-input amplifier, and having a body terminal coupled to the collector terminal of the fifth NPN bipolar transistor;

a fifth PNP bipolar transistor having an emitter terminal coupled to a current source, having a collector terminal coupled to the collector terminal of the third NPN bipolar transistor, and having a body terminal coupled to a first input terminal of the dual differential-input amplifier;

a sixth PNP bipolar transistor having an emitter terminal coupled to the current source, having a collector terminal coupled to the collector terminal of the fourth NPN bipolar transistor, and having a body terminal coupled to a second input terminal of the dual differential-input amplifier;

a seventh NPN bipolar transistor having an emitter terminal coupled to a current sink that draws a current of approximately equal magnitude to a current supplied by the current

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source, having a collector terminal coupled to the collector terminal of the second PNP bipolar transistor, and having a body terminal coupled to the second input terminal of the dual differential-input amplifier; and

an eighth NPN bipolar transistor having an emitter terminal coupled to the current sink, having a collector terminal coupled to the collector terminal of the third PNP bipolar transistor, and having a body terminal coupled to the first input terminal of the dual differential-input amplifier.

20. A circuit in accordance with Claim 19, further comprising an inverter that comprises the following:

a ninth NPN bipolar transistor having an emitter terminal coupled to the low voltage source, having a collector terminal coupled to an output terminal of a comparator, and having a body terminal coupled to the output terminal of the dual differential-input amplifier; and

a seventh PNP bipolar transistor having an emitter terminal coupled to the high voltage source, having a collector terminal coupled to the output terminal of the comparator, and having a body terminal coupled to the output terminal of the dual differential-input amplifier.

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